WHAT IS CLAIMED IS:

1. A semiconductor device having an electrode formed on a surface of a semiconductor substrate, wherein said electrode includes a barrier layer consisting of amorphous or microcrystal expressed by an expression of $M1_xM2_{1-x}(0 < x < 1)$,
where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, Tu, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb.

2. A semiconductor device according to Claim 1, wherein composition ratio of said barrier layer is determined so that grain boundary becomes amorphous to an extend such that at least any one of diffusion of oxygen and spike can be prevented.

3. A semiconductor device according to Claim 1, wherein said surface of semiconductor substrate is a tungsten plug formed on the semiconductor substrate.

4. A semiconductor device according to Claim 1, wherein said surface of semiconductor substrate is formed by material which promotes oxidation at crystallization temperature of a dielectric layer to be formed on said surface of semiconductor.

5. A semiconductor device according to Claim 1, wherein said surface of semiconductor substrate is formed by at

least one kind of polysilicon, tungsten, cobalt, molybdenum, copper, silicide of these, and alloy of these.

6. A semiconductor device according to any one of Claims 1 to 5,

wherein a dielectric layer is formed on said surface of electrode.

7. A semiconductor device according to any one of Claims 1 to 5,

wherein said dielectric layer is PZT.

8. A semiconductor device comprising:

a lower electrode formed on a semiconductor substrate;

a dielectric layer formed on said lower electrode and constructed by ferroelectric or dielectric having high dielectric constant; and

an upper electrode formed on said dielectric layer,

wherein said lower electrode includes a barrier layer consisting of amorphous or microcrystal expressed by an expression of $M1_xM2_{1-x}$ $(0 < x < 1)$,

where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, Tu, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb.

9. A semiconductor device according to Claim 8,

wherein said barrier layer consists of iridium tantalum layer Ir_xTa_{1-x} $(0 < x < 1)$.

10. A semiconductor device according to Claim 8, wherein said barrier layer includes a grading layer in which a composition ratio is changed.

11. A semiconductor device according to Claim 8, wherein said barrier layer consists of iridium tantalum layer Ir_xTa_{1-x} $(0 < x < 1)$ and material of said electrode is iridium.

12. A semiconductor device according to Claim 8, wherein said barrier layer consists of iridium tantalum layer Ir_xTa_{1-x} $(0 < x < 1)$ and material of said electrode is platinum.

13. A semiconductor device comprising:

a lower electrode formed on a semiconductor substrate;

a dielectric layer formed on said lower electrode and constructed by ferroelectric or dielectric having high dielectric constant; and

an upper electrode formed on said dielectric layer,

wherein said electrode includes between said dielectric layer and said upper electrode a barrier layer consisting of amorphous or microcrystal expressed by an expression of $M1_xM2_{1-x}$ $(0 < x < 1)$, where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re,

Rh, Tu, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb.

14. A semiconductor device according to Claim 13, wherein said barrier layer consists of iridium tantalum layer Ir_xTa_{1-x} $(0 < x < 1)$.

15. A semiconductor device having an electrode formed on a surface of a semiconductor substrate, wherein said electrode is constructed by amorphous or microcrystal single layer expressed by an expression of $M1_xM2_{1-x}$ $(0 < x < 1)$, where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, Tu, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb.

16. A semiconductor device according to Claim 1, wherein said barrier layer includes of constructive element of substrate material.

17. A method for manufacturing a semiconductor device comprising a first process forming an electrode formed on surface of a semiconductor substrate and a second process forming a dielectric film on the upper layer thereof, wherein said first process includes a process forming a barrier layer consisting of amorphous or microcrystal expressed by an expression of $M1_xM2_{1-x}$ $(0 < x < 1)$, where

M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, Tu, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb.

18. A method for manufacturing a semiconductor device according to Claim 17,

wherein composition ratio of said barrier layer is determined so that grain boundary becomes amorphous in degree enabling to prevent diffusion of oxygen or spike and forming process of said dielectric layer is process forming film at lower temperature than crystallization temperature of said barrier layer.

19. A method for manufacturing a semiconductor device according to Claim 17,

wherein said electrode is formed on a tungsten plug formed on surface of the semiconductor substrate.

20. A method for manufacturing a semiconductor device according to Claim 17,

wherein at least surface layer of said electrode is formed on material which promote oxidation at crystallization temperature of a dielectric layer to be formed on said surface of semiconductor.

21. A method for manufacturing a semiconductor device according to Claim 17,

wherein said electrode is formed by at least one of polysilicon, tungsten, cobalt, molybdenum, copper, these silicide, and these alloy.

22. A method for manufacturing a semiconductor device according to any of one of Claims 17 to 21,
wherein said dielectric layer is a ferroelectric layer.

23. A method for manufacturing a semiconductor device according to any of Claim 17 to Claim 21,
wherein a forming process of said ferroelectric layer is a process forming PZT by Sol-Gel method.

24. A method for manufacturing a semiconductor device including:
process forming a lower electrode on surface of a semiconductor substrate;
process forming a dielectric layer consisting of ferroelectric or dielectric having high dielectric constant on said lower electrode; and
process forming an upper electrode on said dielectric layer,
wherein said process forming the lower electrode includes process forming a barrier layer consisting of amorphous or microcrystal expressed by an expression of $M1_xM2_{1-x}$ $(0 < x < 1)$ so as to form a dielectric capacitor, where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, Tu, Cu, Co, Fe, Ni, V, and Cr, and

M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb.

25. A method for manufacturing a semiconductor device according to Claim 24,

wherein said barrier layer consists of iridium tantalum layer Ir_xTa_{1-x}.

26. A method for manufacturing a semiconductor device including:

process forming a lower electrode on a semiconductor substrate;

process forming a dielectric layer consisting of ferroelectric or dielectric having high dielectric constant on said lower electrode;

process forming a barrier layer consisting of amorphous or microcrystal expressed by an expression of $M1_xM2_{1-x}$ $(0 < x < 1)$ on said dielectric layer, where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, Tu, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb; and

process forming an upper electrode on said barrier layer so as to form a dielectric capacitor.

27. A method for manufacturing a semiconductor device according to Claim 26,

wherein said barrier layer consists of iridium tantalum layer Ir_xTa_{1-x}.

28. A method for manufacturing a semiconductor device according to Claim 26,

wherein said process forming the barrier layer includes spattering process forming grading layer by varying target temperature and varying composition ratio gradually.

29.A method for manufacturing a semiconductor device comprising an electrode formed on surface of a semiconductor substrate, wherein said electrode is constructed by amorphous or microcrystal single layer expressed by an expression of $M1_xM2_{1-x}$ $(0 < x < 1)$, where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, Tu, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb.

30.A method for manufacturing a semiconductor device according to Claim 17,
wherein said barrier layer includes constructive element of substrate material.

31. A semiconductor device having an electrode formed on a surface of a semiconductor substrate,
wherein said electrode includes an amorphous or microcrystal barrier layer which includes at least an element chosen from a first group of Au, Pt, Ir, Pd, Os, Re, Rh, Tu, Cu, Co, Fe, Ni, V and Cr and at least an element chosen from a second group of Ta, Ti, Zr, Hf, W, Y, Mo and Nb.

32. A semiconductor device according to claim 31, wherein said barrier layer is made of IrTaPt.